ROEE KALINSKY

Electrical Engineer, Independent Contractor
Specializing in FPGA, ASIC, and Embedded Systems Design

Doing business as Porcupine Technology LLC
Tel: 858.472.3079 ● E-mail: roee@porcupinetech.com ● Web: http://www.porcupinetech.com
11908 Tivoli Park Row, Unit 7 ● San Diego, CA 92128

AREAS OF EXPERTISE

Technologies

- Wireless communications
- Networking
- Digital video
- Embedded systems

FPGA & ASIC Design

- System architecture, high-level and detailed design, interface design
- Mapping system requirements and algorithms into hardware-efficient designs
- RTL development
- VHDL and Verilog
- Evaluation and integration of 3rd party IP
- Functional verification, self-checking test bench development, test case development
- Methodologies that maximize design efficiency, robustness, and maintainability/reuse
- Timing and physical constraints development, synthesis, place & route, static timing analysis
- Extensive experience with Xilinx and Altera FPGA devices and development tools
- Other architectures and tool chains including Modelsim, Synplicity, Synopsys, ISE, Vivado, Quartus

Board-Level Hardware Design

- High-speed digital and mixed signal design
- Experience with various microprocessor families, memory technologies, busses, and I/O standards
- Efficiently bringing up and debugging prototype hardware in a lab environment

Programming & Software Design

- C, C++, Ruby, Perl, Tcl, shell scripting, Matlab/Octave, assembly
- Object-oriented programming
- Embedded systems programming, event driven software and real-time multitasking / RTOS

Other Skills

- Excellent problem solving skills
- Proficient with UNIX/Linux and Microsoft environments
- Bilingual: English & Hebrew
- Private pilot, instrument rated
- Amateur designer/builder of experimental aircraft and avionics systems

Please see the following pages for a detailed history of professional experience.

PROFESSIONAL EXPERIENCE

Independent Contractor (doing business as Porcupine Technology LLC)

Part time since 1999, full time April 2002 to Present (as Porcupine Technology LLC since 2009)
Projects listed below in reverse chronological order

Adaptive Dynamics – FPGA IP for interference mitigation in wireless receivers

- Evaluated client's canonical algorithms and developed modifications to them that reduced hardware resource utilization by greater than a factor of thirty with no loss in algorithm performance. Contributed additional changes to further improve algorithm performance while maintaining hardware efficiency.
- Developed an FPGA core implementing the above algorithms (coded in plain VHDL) that is highly configurable/scalable to accommodate a wide range of different target systems and applications.
- Developed and employed methods to make the core design independent of any specific FPGA device architecture, while making provisions to ensure that it can map to all modern Xilinx and Altera FPGA device families in a timing and resource-efficient manner. Supported devices included Xilinx Virtex-4 through Kintex-7 and Ultrascale, and Altera Cyclone 3 through Stratix and Arria 10.
- Developed processes for end-to-end design verification across multiple disciplines within the company, connecting the dots between Matlab and full precision C models produced by the systems and software teams, to VHDL and corresponding bit-accurate C models produced by the FPGA team.
- Developed automated tool flows and other essential design processes to make the client's design activities far more effective and robust.
- Provided leadership to other engineers in algorithm development, FPGA development, and integration.

Serrano Systems, Acorn Technologies – FPGA/ASIC IP for 4G LTE & WiMAX PHY layer

- Developed IP to improve OFDM receiver performance via a novel approach to time domain channel estimation. Specific designs targeted LTE and WiMAX.
- Contributed to algorithm development, modeling, and evaluation of performance and implementation feasibility.
- Mapped theoretical/mathematical models and algorithms into hardware-efficient designs. Evaluated performance and architectural trade-offs. Implemented designs as Verilog IP cores for ASIC and FPGA targets plus supporting software components.
- Developed self-checking verification environments for Matlab and Verilog models.
- Performed additional lab testing using an FPGA-based platform.

Intellisis – Neural network processor architecture study

- Evaluated possible architectures for mapping a certain class of neural network algorithms to silicon.

Client confidential – 4K digital cinema camera

- System architect. Worked with the client on requirements definition and specification development. Created the high-level design for the camera, then the FPGA high-level and detailed design. Worked closely with my software counterparts and other key colleagues in evaluating architectural trade-offs.
- Tech lead of the FPGA team, which averaged about six engineers throughout the project. Established design guidelines and methodologies, and developed custom automated design flows where existing ones were inadequate. Personally implemented many of the key FPGA modules, while providing oversight and guidance to the other team members as they implemented other portions of the design.
- The design utilized two Xilinx Virtex-4 FPGAs, and made use of the Virtex-4's advanced features including the embedded PowerPC cores, DSP cores, advanced clocking resources, and Rocket I/O. The most interesting design features are unfortunately confidential at this time.

Vativ Technologies – HDMI receiver ASIC functional verification

- Created a high-level test bench environment for end-to-end verification of the audio and video data paths and protocols. Implemented using an object-oriented high level language operating over Verilog PLI.
- Created directed test cases as well as constrained-randomized tests that identified bugs and specification issues not detected by existing block-level test benches.
- Assisted in porting the digital section of the ASIC to a Xilinx FPGA for early prototyping.

Path 1 Network Technologies – Video-over-IP gateway

- Performed system-level design and FPGA development (targeting a Xilinx Virtex-4).
- Evaluated and integrated third-party cores for standard interfaces, including SPI-4, HD-SDI, and Gigabit Ethernet.

(continued next page)

Independent Contractor (contd.)

Wind River – Fibre Channel extender architecture study

- Created an architecture for a device that extends the capabilities of Fibre Channel for a particular environment. A design based on my architecture was then successfully implemented by the client.

Wind River, Redlake – HG-TH tethered-head high-speed digital video camera

- Developed a proprietary network architecture, layers 1 through 4, tailored to the unique functional, physical, and economic requirements of this camera system (no existing standard at the time met the req's).
- Features included a packet-switched ring-star topology, per-segment bandwidth scalability, fault tolerance, streaming as well as reliable asynchronous transport types, QoS provisions, virtual interrupts, and timebase distribution. Physical layer built on Xilinx Rocket I/O technology. Implemented the network components and the functional verification environment in VHDL. Targeted the design for Xilinx Virtex-II Pro FPGAs.
- Provided technical leadership to other FPGA developers on the project.
- Played lead role in integration and debug of the system FPGAs, encompassing many other functional areas including image processing, memory controllers, Gigabit Ethernet, and digital PLL.
- Made improvements to client's tool flow and timing constraint strategies, resulting in greatly improved device utilization and reliability.

Ceyx Technologies – CCFL control demo

- Implemented a PWM-based intensity controller for a cold cathode lamp. Implemented in Verilog, and prototyped on a Xilinx Spartan-3 FPGA development board.

Path 1 Network Technologies – ASI I/O for Video over IP gateway

- Analyzed and improved an existing design for configurable ASI I/O, to bring it into standards compliance. Made circuit and layout changes, and then verified compliant circuit performance on the revised hardware.

Wind River, Redlake – HG-100K high-G high-speed digital video camera

- Designed a bus architecture and specialized DMA engines for transport and synchronizing of image, calibration, and control data between FPGAs residing on five cards interconnected through a backplane. Implemented in VHDL, targeted for Xilinx Virtex-II FPGAs.

Xsilogy – Internet gateway for remote sensor networks

- Performed independent design reviews of embedded systems hardware and programmable logic.

Tel Aviv University – software for cochlear implant research (unpaid volunteer work)

- Provided technical consultation on recording, synthesis, and digital processing of audio signals to support a set of studies conducted by an audiology researcher.
- Created a set of multimedia Windows applications that interact with human test subjects for various experiments. Implemented using Visual C++.
- Assisted in the organization, analysis, and graphical depiction of test data using Matlab and Excel.

Quantum Think Group, Inc. (a.k.a. QThink), San Diego, CA

Senior Design Engineer - January 2001 to April 2002

Controller ASIC for mass storage device

- Redesigned critical areas of the client's existing data compression and decompression engines for greater performance and robustness in a next generation ASIC.
- Developed an automated script-based flow for the client's front end tools.

3G wireless System on Chip ASIC integration

- Assisted the client with integration of an Oak DSP core and other third party IP into an AMBA-based wireless communication SoC.

(continued next page)

QThink (contd.)

AMBA toolkit

- Independently developed an AMBA toolkit from the bus specification. It included bus functional models, monitors, protocol checkers, bus agents, and central resources. Implemented in Verilog.

Used the toolkit to create a simple AMBA-based reference design.Library qualification suite

- Designed a program capable of analyzing various file types of a standard cell ASIC library for correctness, completeness, and consistency. Implemented in Perl.

Design methodology

- Developed and documented design practices and methodologies. Developed training materials and mentored other engineers in theory and practice of HDL-based design.

Doctor Design, Inc. / Wind River Services, San Diego, CA

Senior Design Engineer - September 2000 to January 2001
Design Engineer - June 1999 to September 2000
Associate Engineer (student intern) - October 1997 to June 1999

12 GIPS high-availability packet processing platform

- Designed two types of quad-CPU cards and a backplane. The design used 64-bit MIPS CPUs, high-performance memory systems, bridged multi-tiered PCI, I2O messaging, and Ethernet.

DVR reference design

- Developed algorithms for real-time manipulation of MPEG-2 transport streams. Modeled in C++, then in VHDL, and emulated in real time using Altera FPGAs.
- Evaluated the relative performance of several available MPEG encoder and decoder chips.
- Designed board-level hardware and programmable logic for a DVR reference design.

Ceiva Digital Photo Receiver, "world's first Internet-connected picture frame"

- Led the hardware design from feasibility study through architecture, board design, bring-up, integration, regulatory compliance testing (FCC and UL), and transition to manufacturing.

Telxon wireless industrial mobile computers

- Designed various peripherals and external interfaces to PC/AT compatible standards.
- Designed hardware and firmware for power management, including power control of individual subsystems and charge management for lithium ion and NiCd batteries.
- Played a leading role in systems integration and debug.

And more…

- Participated in the design of numerous set-top boxes, Internet appliances, wireless PDAs, and other “smart” devices.

FORMAL EDUCATION

University of California, San Diego

Bachelor of Science Electrical Engineering - June 1999
Cum Laude